

# FQA18N50V2

## 500V N-Channel MOSFET

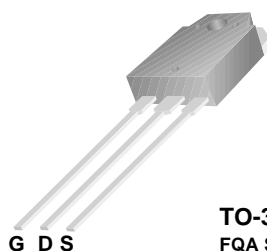
### General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

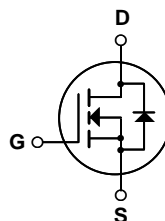
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies, active power factor correction, electronic lamp ballast based on half bridge topology.

### Features

- 20A, 500V,  $R_{DS(on)} = 0.265\Omega$  @  $V_{GS} = 10V$
- Low gate charge ( typical 42 nC)
- Low  $C_{rss}$  ( typical 11 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



**TO-3P**  
**FQA Series**



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FQA18N50V2	Units
$V_{DSS}$	Drain-Source Voltage	500	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ )	20	A
	- Continuous ( $T_C = 100^\circ\text{C}$ )	12.7	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	80	A
$V_{GSS}$	Gate-Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	330	mJ
$I_{AR}$	Avalanche Current (Note 1)	20	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	27.7	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ )	277	W
	- Derate above $25^\circ\text{C}$	2.22	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	0.45	$^\circ\text{C/W}$
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink	0.24	--	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	40	$^\circ\text{C/W}$

**Electrical Characteristics** $T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	500	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.5	--	V/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	$\mu\text{A}$
		$V_{DS} = 400\text{ V}, T_C = 125^\circ\text{C}$	--	--	10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

**On Characteristics**

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3.0	--	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	--	0.225	0.265	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 10\text{ A}$ (Note 4)	--	16	--	S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	2530	3290	pF
$C_{oss}$	Output Capacitance		--	300	390	pF
$C_{rss}$	Reverse Transfer Capacitance		--	11	14.3	pF
$C_{oss}$	Output Capacitance	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	76	--	pF
$C_{oss\text{ eff.}}$	Effective Output Capacitance	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$	--	150	--	pF

**Switching Characteristics**

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250\text{ V}, I_D = 18\text{ A},$ $R_G = 25\text{ }\Omega$  (Note 4, 5)	--	40	90	ns
$t_r$	Turn-On Rise Time		--	150	310	ns
$t_{d(off)}$	Turn-Off Delay Time		--	95	200	ns
$t_f$	Turn-Off Fall Time		--	110	230	ns
$Q_g$	Total Gate Charge	$V_{DS} = 400\text{ V}, I_D = 18\text{ A},$ $V_{GS} = 10\text{ V}$  (Note 4, 5)	--	42	55	nC
$Q_{gs}$	Gate-Source Charge		--	12	--	nC
$Q_{gd}$	Gate-Drain Charge		--	14	--	nC

**Drain-Source Diode Characteristics and Maximum Ratings**

I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		--	--	20	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		--	--	80	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 20 A	--	--	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 18 A,	--	420	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge	di <sub>F</sub> / dt = 100 A/μs (Note 4)	--	5.4	--	μC

**Notes:**

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2.  $L = 1.83\text{ mH}, I_{AS} = 18\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\text{ }\Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 18\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$
5. Essentially independent of operating temperature

## Typical Characteristics

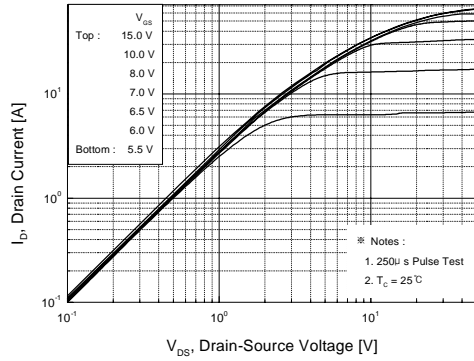


Figure 1. On-Region Characteristics

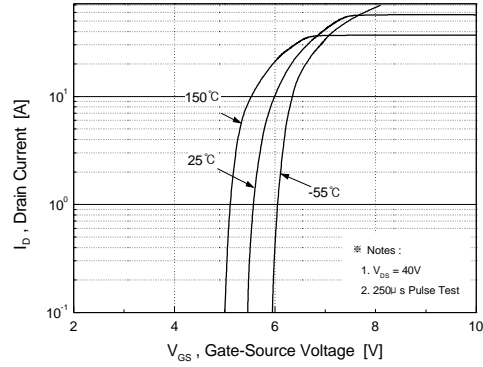


Figure 2. Transfer Characteristics

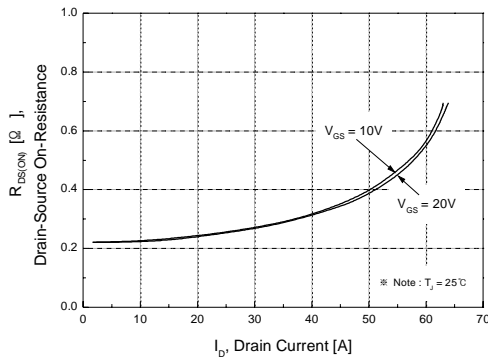


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

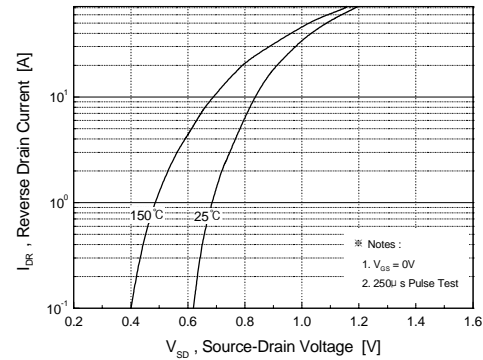


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

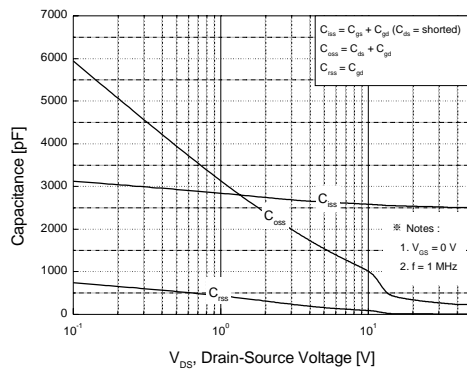


Figure 5. Capacitance Characteristics

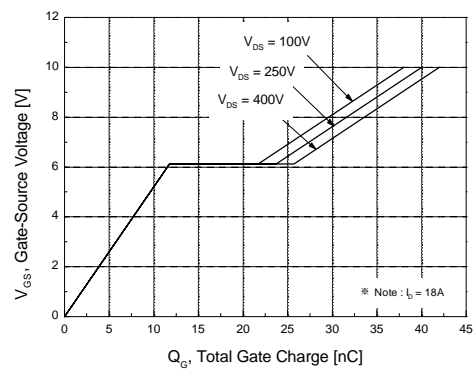
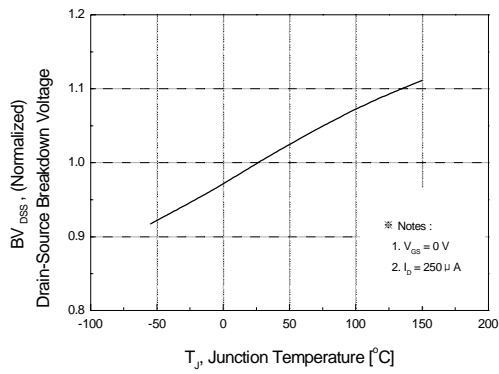
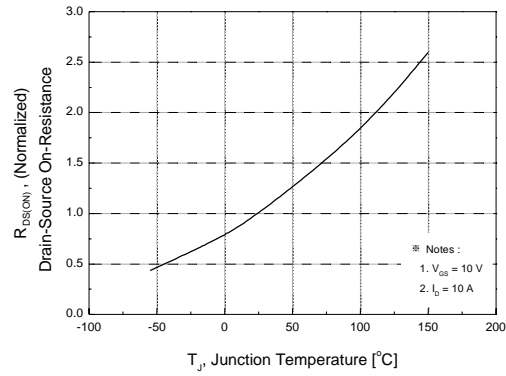


Figure 6. Gate Charge Characteristics

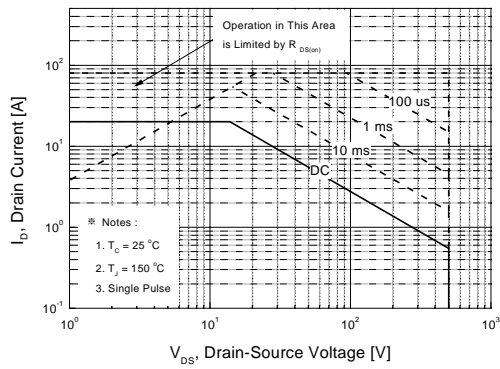
## Typical Characteristics (Continued)



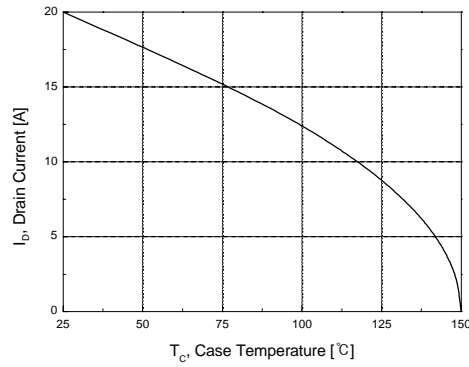
**Figure 7. Breakdown Voltage Variation vs. Temperature**



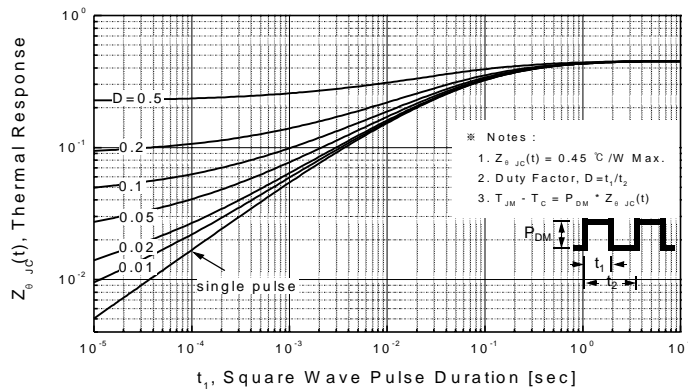
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**

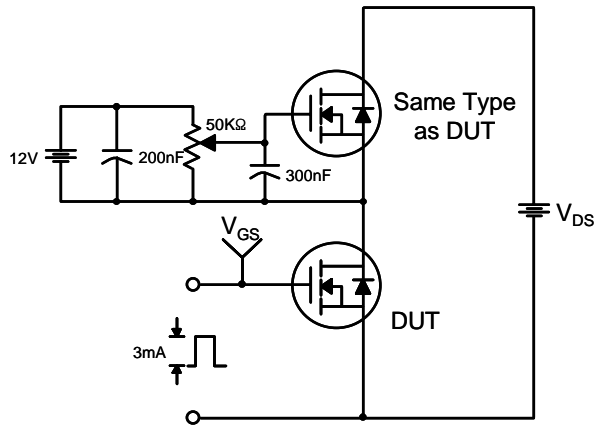


**Figure 10. Maximum Drain Current vs. Case Temperature**

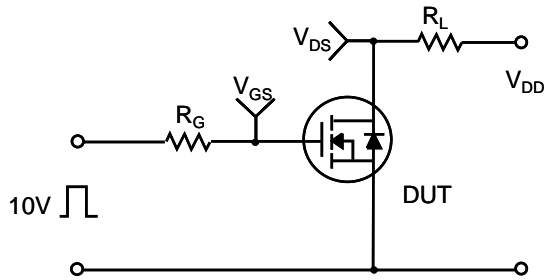


**Figure 11. Transient Thermal Response Curve**

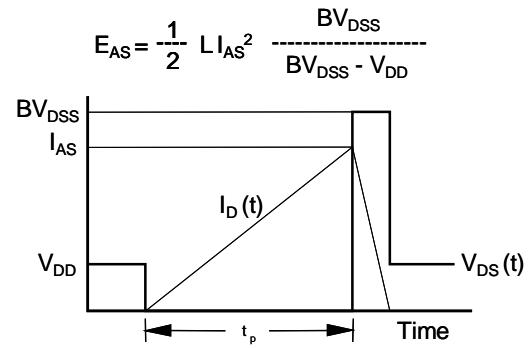
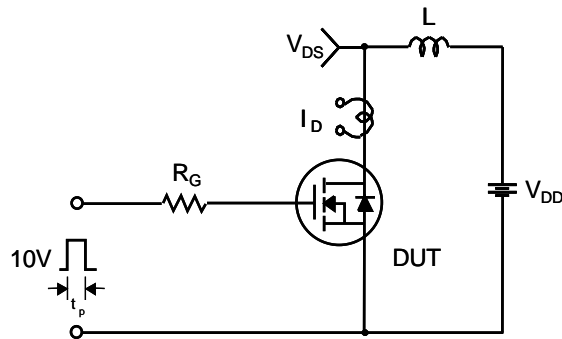
### Gate Charge Test Circuit & Waveform



### Resistive Switching Test Circuit & Waveforms



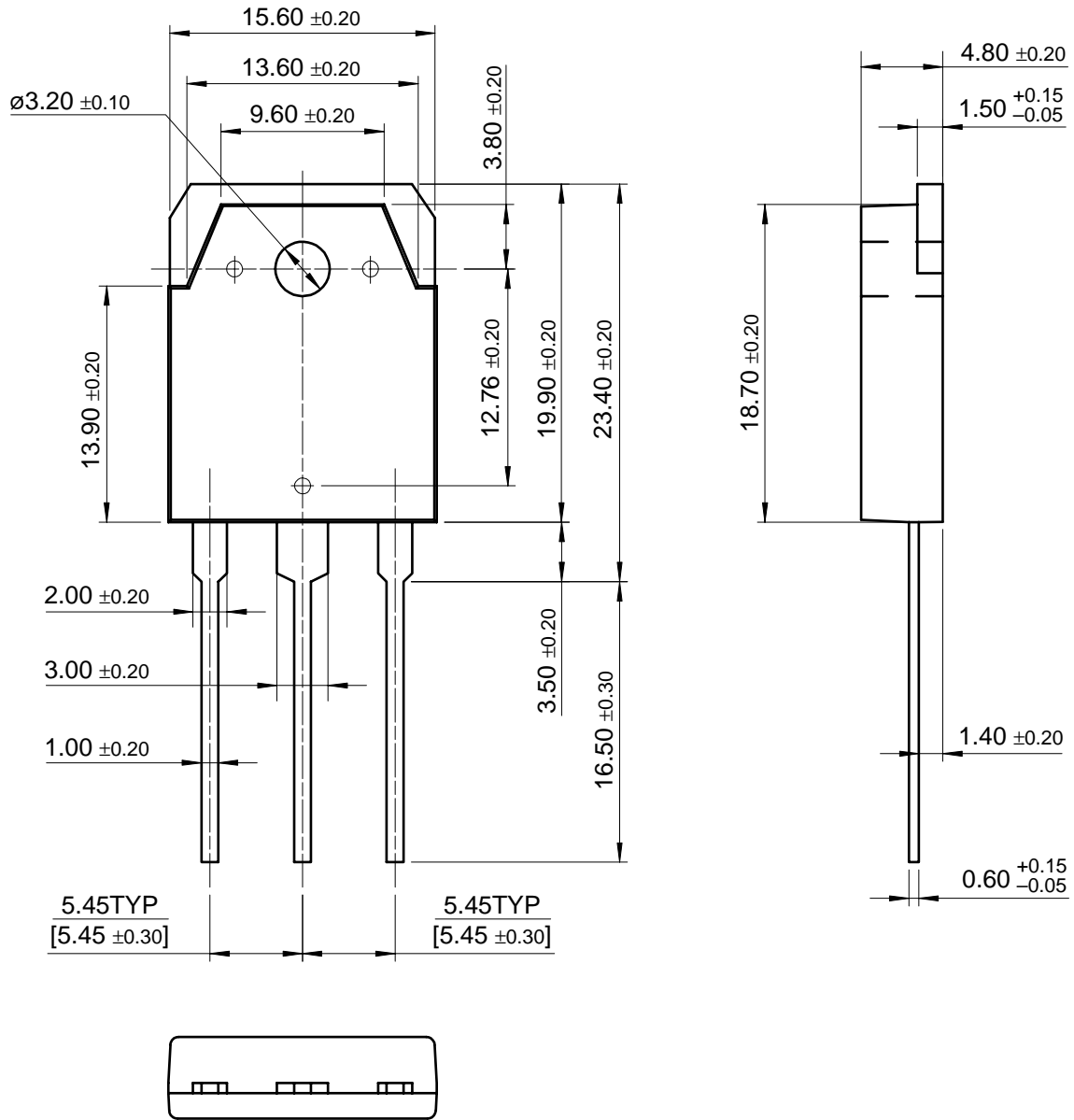
### Unclamped Inductive Switching Test Circuit & Waveforms





## Package Dimensions

TO-3P



Dimensions in Millimeters

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